b) for each combination of said slots, identifying the edges intersected by the connection graph or graphs for that particular combination of slots, wherein a plurality of the identified edges are diagonal; and

c) storing the plurality of identified edges for each combination of slots in a storage structure.

68. (Amended) The method of claim 67, wherein a plurality of the edges are horizontal, and a plurality are vertical.

REMARKS

Reconsideration of the patent application in view of the preceding amendments and the following remarks is respectfully requested.

I. Objection To The Drawings

In the office action dated November 7, 2002, the Draftsperson objected to the drawings. Specifically, the Draftsperson stated that the top margin for **Figures 3, 25, 27, 29, 30A, 34, 37, 39, 40, 43** and **48B** were not acceptable. Applicants have resubmitted the subject figures with corrected margins and respectfully request approval of them.

II. Objection To The Specification

In the office action dated November 7, 2002, the Examiner objected to the title of the application due to a hyphen between the words "Integrated" and "Circuit." With this Response, Applicants have replaced the title such that the hyphen no longer appears.

III. Objection To The Claims

In the office action dated November 7, 2002 the Examiner objected to claims 28, 43, 58, and 67 due to two types of informalities: claims 58 and 57 contained a hyphen between the words "IC" and "layout"; and, claims 28, 43, 58, and 67 referred to "**the** topology of interconnect lines" rather than "**a** topology of interconnect lines." Applicants have corrected these informalities through amendment to the subject claims.

IV. Rejection of the Claims Under 35 U.S.C. § 112, second paragraph

In the office action dated November 7, 2002 the Examiner rejected claims under 35 U.S.C. § 112, second paragraph. Specifically, the Examiner rejected claims 28, 29, 43, 44, 58, 59, 67 and 68 due to the use of the word "some" in referencing the use of edges or line paths. Claims 28, 31, 43, 58, and 67 were further rejected as being unclear with respect to the nature of particular elements.

Applicants have amended claims 28, 29, 43, 44, 58, 59, 67, and 68 to recite "a plurality" rather than "some." These amendments are fully supported by the specification as originally filed, for example at **Figures 13-15** and at Figures **24-29**. Applicants respectfully submit that the amendments obviate the Examiner's rejections.

Applicants have further amended claims 28, 31, 43, 58, and 67 as follows: claim 28 now recites "d) identifying the edges, from a plurality of edges, . . ."; claim 31 now recites "the plurality of edges . . ."; claim 43 now recites "d) identifying the plurality of line paths . . ."; claim 58 now recites "c) storing the plurality of identified line paths . . ."; and, claim 67 now recites "c) storing the plurality of identified edges . . ." Applicants respectfully submit that the amended claims are definite under 35 U.S.C. § 112.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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THE AMENDED CLAIMS

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

28. (Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions, wherein a plurality of edges exist between said sub-regions, wherein [some] a plurality of said edges are diagonal;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the edges, from the plurality of edges, intersected by at least one connection graph that represents [the] a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified edges is diagonal; and

e) computing a placement cost by using the identified edges.

29. (Amended) The method of claim 28, wherein [some] a plurality of said edges are horizontal and [some] a plurality are vertical.

31. (Amended) The method of claim 30, wherein the plurality of edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines.

43. (Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) partitioning the IC region into several sub-regions, wherein a plurality of line paths exist between said sub-regions, wherein [some] a plurality of said line paths are diagonal;

b) selecting a net;

c) identifying the set of sub-regions containing the circuit elements of the selected net;

d) identifying the plurality of line paths used by at least one connection graph that represents [the] a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified line paths is diagonal; and

e) computing a placement cost by using the identified line paths.

44. (Amended) The method of claim 43, wherein [some] a plurality of said line paths are horizontal and [some] a plurality are vertical.

58. (Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of line paths exist between said slots, a method of pre-computing costs of placing circuit modules in an IC layout region, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that represents [the] a topology of interconnect lines necessary for connecting the combination of said slots;

b) for each combination of said slots, identifying the line paths used by the connection graph or graphs for that particular combination of slots, wherein [some] a plurality of the identified line paths are diagonal; and

c) storing the plurality of identified line paths for each combination of slots in a storage structure.

59. (Amended) The method of claim 58, wherein [some] a plurality of the line paths are horizontal, and [some] a plurality are vertical.

67. (Amended) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, wherein a plurality of edges exist between said slots, a method of pre-computing costs of placing circuit modules in an IC layout region, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that represents [the] a topology of interconnect lines necessary for connecting the combination of said slots;

b) for each combination of said slots, identifying the edges intersected by the connection graph or graphs for that particular combination of slots, wherein [some] a plurality of the identified edges are diagonal; and

c) storing the plurality of identified edges for each combination of slots in a storage structure.

68. (Amended) The method of claim 67, wherein [some] a plurality of the edges are horizontal, and [some] a plurality are vertical.